# A D-band Dual-Mode Dynamic Frequency Divider in 130nm SiGe Technology 

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TABLE I
RECENTLY REPORTED FREQUENCY DIVIDERS


#### Abstract

In this work, a dual-mode (divide-by-2 and divide-by-3) dynamic frequency divider is presented. A tunable delay gated ring oscillator (TDGRO) topology is proposed for dual-mode operation and bandwidth extension. It uses a 130 nm gate length SiGe BiCMOS technology with $f_{t}$ and $f_{\text {max }}$ of $250 \mathbf{~ G H z}$ and 370 GHz , respectively. Verification shows that it works at W -band from 70 GHz to 114 GHz ( $\mathbf{4 7 . 8 \%}$ bandwidth) for divide-by- 2 and works at D-band from 105 GHz to $160 \mathrm{GHz}(41.5 \%$ bandwidth) for divide-by-3. This divider can be used in integrated phase lock loops (PLLs) at millimeter-wave frequencies.


Index Terms-dynamic, frequency divider, SiGe, BiCMOS, Dband, W-band, millimeter-wave, dual-mode

## I. Introduction

Millimeter-wave and THz bands offer wide bandwidth for high-speed communication systems. In a millimeter-wave communication system, high-frequency synthesizer (e.g., phase-locked loop) and carrier recovery blocks are essential parts at the receiver side. The frequency divider, voltagecontrolled oscillators and phase detectors are critical components of a millimeter-wave frequency synthesizer.

A dual-mode divider that can divide the input frequency either by- 2 or by- 3 can offer flexibility for millimeter-wave band synthesizer as the first divider stage. It allows a wide input frequency range to be converted into the same output frequency band, so it is less demanding on the bandwidth of the subsequent divider stage. Dual-mode operation is often implemented with tunable capacitors included in the injection locked frequency divider circuit. In paper [1], a pair of switched capacitors are used as a capacitive load. When the switched capacitor is by-passed, the divider is in the divide-by- 2 mode. When the switch is on, the capacitor shifts the resonator frequency of the tank, so the divider is switched to divide-by-3 mode. The dual-mode operation can also be made by changing varactors [2-4], active inductance [5].

For previously reported dual-modulus dividers, their locking range is often narrow (several GHz ) and their input frequencies are relatively low (below 20 GHz ). For divide-by- 3 only

[^0]| Ref | Technology | Frequency range <br> $(\div 2)(\mathrm{GHz})$ | Frequency range <br> $(\div 3)(\mathrm{GHz})$ | $P_{D C}$ <br> $(\mathrm{~mW})$ |
| :---: | :---: | :---: | :---: | :---: |
| $[1]$ | $0.18 \mu \mathrm{~m}$ CMOS | $3.44 \sim 5.02(37.4 \%)$ | $4.28 \sim 4.81(11.7 \%)$ | 3.15 |
| $[2]$ | $0.35 \mu \mathrm{~m}$ CMOS | $4.56 \sim 5.59(20.3 \%)$ | $6.94 \sim 8.41(19.2 \%)$ | 15.2 |
| $[3]$ | $0.18 \mu \mathrm{~m}$ CMOS | $3.18 \sim 4.05(24 \%)$ | $4.85 \sim 5.7(16.1 \%)$ | 12.5 |
| $[4]$ | $0.18 \mu \mathrm{~m}$ CMOS | $8.42 \sim 10.95(26 \%)$ | $13.66 \sim 16.03(16 \%)$ | 4.17 |
| $[5]$ | $0.35 \mu \mathrm{~m}$ CMOS | $1.5 \sim 2.05(31 \%)$ | $1.74 \sim 1.95(11.4 \%)$ | 1.49 |
| $[6]$ | $0.18 \mu \mathrm{~m}$ CMOS | $5.37 \sim 7.68(35.4 \%)$ | $8.07 \sim 11.4(34.2 \%)$ | 3 |
| $[7]$ | $0.18 \mu \mathrm{~m}$ BiCMOS | -- | $132.5 \sim 140.4(5.8 \%)$ | 71.2 |
| $[8]$ | 90 nm CMOS | -- | $91.8 \sim 109.8(17.9 \%)$ | 0.13 |
| $[9]$ | 40 nm CMOS | -- | $236.6 \sim 245.2(3.6 \%)$ | 3.3 |
| $[10]$ | 65 mm CMOS | -- | $58.6 \sim 67.2(13.7 \%)$ | 5.2 |
| $[12]$ | $0.13 \mu \mathrm{~m}$ BiCMOS | $47 \sim 217(93.4 \%)$ | -- | 217 |
| $[13]$ | $0.13 \mu \mathrm{~m}$ BiCMOS | $38 \sim 189(133 \%)$ | -- | 217 |
| $[14]$ | $0.13 \mu \mathrm{~m}$ BiCMOS | $6 \sim 75(170 \%)$, | -- | 196 |
| This | $0.13 \mu \mathrm{~m}$ BiCMOS | $70 \sim 114(47.8 \%)$ | $105 \sim 160(41.5 \%)$ | $26 \sim 180$ |

dividers, the highest input frequency reaches D-band; however, the operational bandwidth is smaller than 20 GHz .

In this letter, a tunable delay gated ring oscillator (TDGRO) topology is proposed for dual-mode operation and bandwidth extension. A TDGRO dynamic frequency divider is designed and implemented for both divide-by-2 and divide-by-3, with a wide input frequency range of $70-160 \mathrm{GHz}$. For input frequency between $70-114 \mathrm{GHz}$, the divider operates as divide-by-2, therefore output is in $35-57 \mathrm{GHz}$. For input frequency between $105-160 \mathrm{GHz}$, the divider operates as divide-by-3 and the output is in $35-53.3 \mathrm{GHz}$. By toggling between operation modes, the output frequency lies in the same frequency band for a wide input frequency range. Previously published relevant works [1-10][12-14] are summarized in Table I, the proposed frequency divider demonstrates the highest input frequency ( 160 GHz ) among the dividers that have dual-modulus, divide-by-2 and divide-by-3, and a state-of-the-art operational bandwidth ( $41.5 \%$ ) among divide-by- 3 dividers.

## II. TDGRO DYNAMIC FREQUENCY DIVIDER

A TDGRO dynamic frequency divider topology is proposed in this work. A simplified functional diagram of the proposed TDGRO dynamic frequency divider is shown in Fig. 1. A TDGRO comprises of two gated differential amplifiers
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Fig. 1 A simplified TDGRO frequency divider topology.

(a)

(b)

Fig. 2 An illustration of voltage change of four nodes when (a) divide-by2, and (b) divide-by-3.


Fig. 3 The schematic of the dynamic frequency divider.


Fig. 4 The simulated tunable delay with different bias conditions.
(denoted as Amp1 and Amp2) with feedback connections to form a ring oscillator configuration. The delays between amplifiers, denoted as $\tau$, are tunable with current in order to switch the division modes. The two amplifiers are gated by an input clock voltage, Amp1 and Amp2 are turned on at high/low voltage, respectively. A similar structure has been used in a
divide-by-2 frequency divider [11].
To explain the operation principle of the proposed divider, four nodes A, B, C and D are marked in Fig. 1, which can be either at a high voltage state or a low voltage state. Assum low voltage states at nodes A, B, C, and D as an initial state. With a high clock voltage, Amp1 operates and makes the node B as an opposite state of that at node A with a delay $\tau_{A B}$. This state is passed to node C with a delay $\tau_{B C}$. When a low clock voltage occurs, Amp 2 passes this state to node D with a delay $\tau_{C D}$, and the state is further passed back to node A with another delay $\tau_{D A}$. There is a restriction: the state can only be passed to nodes B and D within the positive and negative clock periods, respectively. Considering the circuit symmetry, assume $\tau_{A B}+$ $\tau_{B C}=\tau_{C D}+\tau_{D A}=\tau, \tau_{A B}=\tau_{C D} \ll \tau_{B C}=\tau_{D A}$.

When divide-by-2, the voltage waveform at input and output nodes (A, B, C, and D) of Amp1 and Amp2 are depicted in Fig. 2a. Every two periods of input clock are divided into four time slots for a clear explanation. To achieve a divide-by-2 function, the state of node A needs to rise and fall within two clock periods (four time slots), which means the falling edge is in slot(4), and the rising edge is in slot(2). The minimum time for node A to change a state is $\tau_{A B}+\tau_{B C}+\tau_{C D}+\tau_{D A}=2 \tau$. The timing constraints can be expressed as $4 \tau \leq 2 T$. As long as $\tau \leq$ $T / 2$, node B and D can always change status during the positive and negative clock period, respectively. The maximum divide-by- 2 operation frequency is:

$$
\begin{equation*}
f_{d i v 2} \leq \frac{0.5}{\tau} \tag{1}
\end{equation*}
$$

For divide-by-3 operation, the voltage waveforms are illustrated in Fig. 2b. Every three periods of input clock are divided into six time slots for a clear explanation. Assum again low voltage at nodes $\mathrm{A}, \mathrm{B}, \mathrm{C}$, and D as an initial state. To achieve divide-by- 3 function, the state of node A needs to rise and fall within three clock periods, which means the falling edge needs to be in the time slot (6), and the rising edge needs to be in the time slot (3). These timing constraints can be expressed as $4 \tau \leq 3 T$. And $\tau$ is bigger than $T / 2$; otherwise, the divider operates divide-by- 2 . As a result, $0.5 T \leq \tau \leq 0.75 T$.

The falling edge of node A is in slot (6), so the falling edge of node $C$ must be before slot (6). The state of node $C$ can only be passed to node D during a negative clock period. In this case, the falling edge of node D is in slot (4), and the rising edge of node D is in slot (2). The timing constraints can be expressed as

$$
\left\{\begin{array}{l}
1.5 T \leq 3 \tau \leq 2 T  \tag{2}\\
2.5 T \leq 4 \tau \leq 3 T
\end{array}\right.
$$

As a result, $0.625 T \leq \tau \leq 0.67 T$. The divided by three frequency range can be written as:

$$
\begin{equation*}
0.625 / \tau<f_{\text {div } 3}<0.67 / \tau \tag{3}
\end{equation*}
$$

From Eq. (1) and Eq (3), it can be seen that for a given delay $\tau$, the maximum working frequency can be improved by a third with the same $\tau$. The delay $\tau$ is limited by the semiconductor process and the layout.

Fig. 3 shows the schematic of the proposed frequency divider. Q1 and Q2 formed Amp 1, gated by Q9. Q3 and Q4 form Amp 2, gated by Q10. Q11~Q13 are the clock input stage, with Q14~Q16 being the complimentary stage. Q5~Q8 are


Fig. 5 A photo of the on-wafer frequency divider ( $530 \mu \mathrm{~m} \times 460 \mu \mathrm{~m}$ ).


Fig. 6 Output signal power and bias conditions over input frequencies. The dashed lines represent the performance of divide-by-2, while the solid lines represent the performance of divide-by-3


Fig. 7 Output signal spectrum of divide-by-3 at 159 GHz and divide-by-2 at 111 GHz with 5 MHz and 70 GHz spans.


Fig. 8 Input power sensitivity curve of the dynamic divider.
emitter followers for inter-amplifier buffer with Q17~Q20 are their current mirrors.

For a bipolar junction transistor, when the current Ic changes, the delay $\tau_{b e}$ between the base and the emitter and $\tau_{b c}$ between the base and the collector are changed accordingly. In this case, the delay between the two latches is tunable. The total delay $\tau$ consist of a tunable delay from transistors and a fixed delay from the inevitable transmission line in layout. The electric delay of the transmission line is 0.4 ps , which is calculated by using HFSS simulation. The tunable delay is estimated by observing the time delay between the signals at the input of the first latch (base of Q1) and the input of the second latch (base of Q4) when the divider is free running. The simulated tunable delay with different bias conditions is shown in Fig. 4. The total delay $\tau$ can be tuned from 3.6 ps to 5.4 ps .

By using different bias voltage of Vee, the working
frequency of the proposed divider is shifted. With a fixed bias point, the output frequency locking range is fixed, which means the input frequency is selected by bias point. With different input frequencies, the division modulus can be chosen by using different bias voltage of Vee. The circuit has only two biases, Vee and Vb , supplied respectively at -3 V and -1.8 V . A photo of the circuit is given in Fig. 5. The chip size is $530 \mu \mathrm{~m} \times 460$ $\mu \mathrm{m}$, including probing pads.

## III. Measurement Results

The circuit is characterized on-wafer using a Cascade MPS150 probe station. The frequency-domain measurement was performed using a Keysight network analyzer (N5247A PNA-X) and VDI millimeter-wave extenders. Single-ended GSG and DC probes with 100 um pitch were used for RF and DC connection, respectively. Three parameters are measured: output power, output spectrum, and input sensitivity.
In Fig. 6, the output power over different input frequencies is represented. The input power is constant -1 dBm . The working frequency range for the proposed frequency divider is 70-160 GHz . By sweeping the bias voltage, the emitter current is changed accordingly. The wide locking bandwidth is covered for both divide-by-2 and divide-by-3 function mode. The bias voltages and currents of the corresponding working frequency are also shown in Fig. 6.

For a single bias point, the widest locking range for divide-by-2 is 17.2 GHz , from 97.4 GHz to 114.6 GHz , when Vee is 3.05 V , and Iee is 50 mA . The widest locking range for divide-by- 3 is 7.2 GHz , from 132 GHz to 139.2 GHz , when Vee $=-2.73$ V , and $\mathrm{Iee}=20 \mathrm{~mA}$.

DC power consumption varies from 26 mW to 180 mW . When the Vee is -2.6 V , and Iee is only 10 mA , the proposed divider gives a low output frequency. For the divide-by- 3 setting, the divider works from 107.4 GHz to 110 GHz . For the divide-by-2 setting, the divider works from 70 GHz to 76.2 GHz .

Fig. 7 shows the measured single-ended output spectrum of the divider in divide-by- 3 and divide-by- 2 mode when the input signal frequency was set at 159 GHz and 111 GHz , respectively. The corresponding input power is -1 dBm and -2.3 dBm . The output spectrum is shown with frequency spans of 5 MHz and 70 GHz . The input power sensitivity curve of the proposed divider is shown in Fig. 8. The solid red curve represents the input sensitivity of divide-by-2, while the blue dashed curve represents the input sensitivity in divide-by- 3 mode.

## IV. CONCLUSION

A TDGRO dynamic frequency divider is demonstrated in this letter. The proposed divider can operate in a divide-by- 2 or a divide-by- 3 mode. The operating frequency ranges are from 70 GHz to 114 GHz and from 105 GHz to 160 GHz for the two modes, respectively. Compared with the recently published frequency dividers given in Table I, the proposed frequency divider demonstrates the highest frequency among the dividers that divide both by-2 and by-3. The proposed divider in divide-by- 3 mode has also the widest bandwidth of 55 GHz .

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